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Routing Techniques in Network-On-Chip Based Multiprocessor-System-on-Chip for IOT: A Systematic Review

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ABSTRACT: Routing techniques (RTs) play a critical role in modern computing systems that use network-on-chip (NoC) communication infrastructure within multiprocessor system-on-chip (MPSoC) platforms. RTs contribute greatly to the successful performance of NoC-based MPSoCs due to traffic congestion avoidance, quality-of-service assurance, fault handling and optimisation of power usage. This paper outlines our efforts to catalogue RTs, limitations, recommendations and key challenges associated with these RTs used in NoC-based MPSoC systems for the IoT domain. We utilized the PRISMA method to collect data from credible resources, including IEEE Xplore ®, ScienceDirect, Association for Computing Machinery and Web of Science. Out of the 906 research papers reviewed, only 51 were considered relevant to the investigation on NoC RTs. The study addresses issues related to NoC routing and suggests new approaches for in-package data negotiating. In addition, it gives an overview of the recent research on routing strategies and numerous algorithms that can be used for NoC-based MPSoCs. The literature analysis addresses current obstacles and delineates potential future avenues, recommendations, and challenges analyzing techniques to assess performance utilizing metrics within the TCCM framework.

Keywords: MPSoC, System-on-Chip, Routing Techniques, TCCM, Routing algorithms, NoC.

1. INTRODUCTION

MPSoC for IoT applications is described as an integrated circuit that includes several processors on one chip, thus facilitating many parallel processes in order to facilitate efficient and time-based data processing [1]. This architecture improves performance and power efficiency, addressing the variety of computational needs that interconnected devices experience in IoT ecosystems. MPSoC platform integrates several processing units, memory and other system components onto one chip [2]. Many IoT applications (refer to Figure 1) involve real–time processing, where data has to be processed, and the result needs to come within limits of time. MPSoCs with hardened real-time processing units and predictable interconnects have the potential to implement time-sensitive tasks like control systems, robotics, and industrial automation efficiently [3]. The NoC is a significant feature of MPSoC platforms [3], [4]. The NoC is a kind of central communication infrastructure that facilitates an effective data transfer and communications process between distinct components in the MPSoC. These components consist of the processors, memory units, accelerators and other functional blocks all combined in one circuit. The NoC router hosts RTs to find the best path for data transmission between IP cores. RTs are a set of rules and logical operations performed by routers to determine the shortest path for delivering data packets from source to destination [5].

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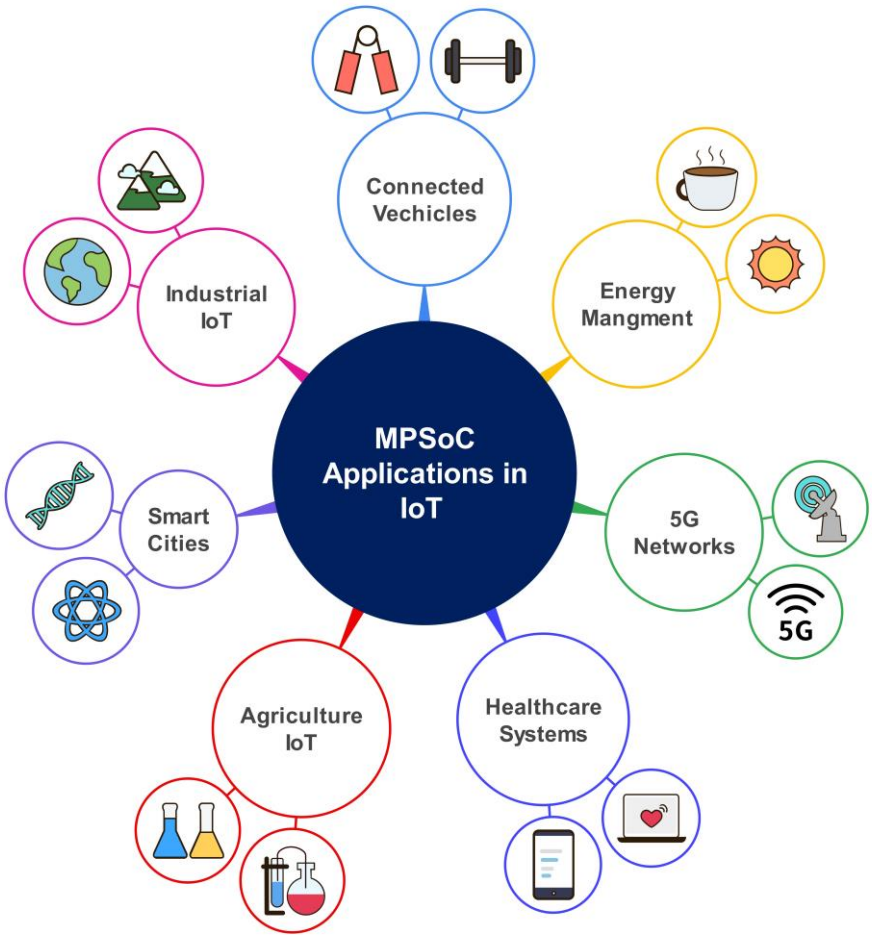

Figure 1. A conceptual model of effective data processing and messaging in real-time situations designed by MPSoC structures created for IoT applications to operate on the basis of time.

Through the widespread use of NoC communication systems, RTs have become an essential part [5], [6]. There is a potential competition in RTs design and implementation extended in fields like NoC-based MPSoC performance [7], [8], security [2], [9], reliability [10], [11], and adaptivity [12]–[14]. RTs control the majority of task mapping and resource sharing in the context of NoC-based MPSoC services [15]. RTs play a critical role in the design and performance of NoC architectures. NoCs have emerged as efficient and scalable interconnection frameworks for MPSoCs. They offer advantages over other forms of MPSoC designs; however, they also present challenges, such as congestion and the impact on performance and efficiency [16]. One of the main key aspects of RTs is addressing congestion within the NoC. Congestion occurs when there is a high volume of network traffic, causing delays and reducing overall system performance [5], [17]. The objective of the comprehensive literature review is to systematically synthesis and analyse current studies on RTs in NoC systems, with a particular emphasis on tackling congestion and optimizing routing decisions.

Several literature studies of RTs for diverse NoC-based MPSoC domain names were formerly published [18], [19]. However, there's nonetheless a scarcity inside the literature that specializes in the RTs-based totally NoC overall performance inside the MPSoC area and diverse venture-mapping and connectivity issues. However, few pieces of literature cover a few components, and an assessment of all factors concerned in RTs-based total overall performance remains scarce. Table 1 depicts how this assessment is different from some of the current literature review papers. Firstly, this overview covers vital factors of RTs in NoC-primarily based MPSoC, which include fault tolerance, workload distribution, and congestion control of NoC communique paths among the source and vacation spot IP cores.

Table 1. Feature-wise comparison of some recent routing techniques review literature with this review.

	Characteristics Covered	[20] 2016	[21] 2017	[22] 2019	[23] 2022	This Review
Based Adaptivity	Mono-objective Routing	✓	✓	×	×	✓
	Multi-objective Routing	✓	×	✓	×	✓
Based Design	Routing Design	×	×	✓	×	✓
	Routing Implementation	×	✓	✓	×	✓
	Routing Utilization	×	✓	✓	×	✓
Based Performance	Latency	×	×	✓	✓	✓
	Throughput	×	×	×	✓	✓
	Security Concerns	×	×	✓	✓	✓
Based Task-Mapping	Livelock Free	✓	×	×	✓	✓
	Deadlock Free	✓	×	✓	✓	✓
	Path Selection	✓	✓	✓	✓	✓
	Network Congestion	×	✓	×	×	✓
	Workload Distribution	×	×	×	×	✓
	Fault Tolerance	✓	✓	×	×	✓
	Congestion Control	×	×	✓	×	✓

The academic literature on RTs is witnessing a consistent expansion, posing challenges in staying abreast of the latest research developments in this field. The research conducted by scholars in the field of MPSoC platforms-based IoT has resulted in significant advancements and extensive scholarly investigations in this domain. Nevertheless, the copious amount of research available presents difficulties in efficiently extracting valuable information from previous studies [24], [25]. As a result, a thorough mapping analysis of routing algorithms was carried out [26]. This study provides a comprehensive review of routing algorithms by employing bibliometric analysis with the aid of the R-tool.

Furthermore, the activity of the systematic analysis plays an essential role in summarising and synthesising results obtained in previous research based on modern knowledge [27]. Moreover, it provides useful advice based on professional experience and wisdom. Therefore, scholars use various methods that take advantage of the already-established body of knowledge to capture and restructure findings from previous scholarly works [24]. Bibliometric analysis is a powerful tool that can provide an unreplaceable and transparent process of review [28], [29]. This was done through scientific activities and statistical measures of knowledge [30], [31].

Using a bibliographic approach in combination with the Theory, Context, Characteristics and Methodology (TCCM) framework, this study creates guidelines for further research applying the TCCM structure [32], [33]. The TCCM structure is one of the most widely used in literature review structures, which researchers would use to find gaps in current studies and suggest future routes for new investigations. It is the first of a series of articles studying and utilizing the TCCM framework [34], [35]. Recent suggestions on systematic literature reviews [36]–[38] advise integrating bibliometric analysis with the TCCM framework to provide comprehensive views. Consequently, this study enriches the existing literature by introducing a comprehensive review. This study presents several noteworthy contributions:

(1) Emphasizing the reorganization of previous literature results, the research provides a comprehensive taxonomy map aligned with current research trends.

(2) The review conducts a thorough examination, summarizing findings from previous literature. Through bibliometric analysis, it illuminates and offers insights, aiding in identifying research gaps within the extensive research stream.

(3) The review actively addresses gaps in the ongoing research literature, contributing significantly by highlighting challenges and recommendations derived from previous literature.
(4) The study identifies potential avenues for further research, emphasizing areas lacking in current research. It offers a comprehensive overview of scientific articles, particularly focusing on automated methods to evaluate various routing algorithms within relevant fields.

2. METHODOLOGY

This section provides a comprehensive explanation of our study of methodology. The methodology of this study is constructed based on the PRESMA approach.

2.1. SEARCH STRATEGY

To accomplish our research goals, we executed a methodical investigation. In light of the conceptual advancements and extensive influx of new information within the realm of RTs, the utilisation of a systematic search methodology has been deemed imperative. In contrast to alternative methodologies, employing a systematic search methodology facilitates the examination of an extensive corpus of data, the detection of disciplinary shifts, the investigation of temporal trends, the provision of a comprehensive panorama of the field, and the provision of valuable insights for both scholars and professionals [24], [39]. In order to conform to the protocols of systematic reviews, the present study adhered to the PRISMA methodology, which advocates for utilising multiple databases. The utilisation of this technique has been documented in prior scholarly works, thereby conforming to the methodology employed in other academic articles [40]–[42]. To facilitate the systematic review process, we acquired subscriptions for Web of Science (WOS), ScienceDirect, Association for Computing Machinery (ACM), and the IEEE Xplore digital library. These platforms included a wide range of journals and conference papers in the domains of Hardware, Embedded Systems, and NoCs, thereby providing a comprehensive perspective on academic research across diverse fields. We also asked expert colleagues from the field of MPSoCs which potential keywords might relate to router algorithms in NoCs. Besides, the reading of existing scholarly works provided a plethora of common keywords such as “routing algorithms”.

2.2. EXCLUSION AND INCLUSION CRITERIA

Whitepapers, webinars and news articles were not considered. The materials are typically not as comprehensive and structured as the in-depth research studies, which makes them less ideal to be included within a systematic literature review [43]. Moreover, to facilitate complete and proper review conduct, only studies that have been provided in the English language are included. Furthermore, only the full-text papers and investigations are considered for inclusion, as they offer sufficient information for a comprehensive analysis. Moreover, the date of publication must be between 2004 and 2023. Finally, investigations that do not align with the topic of study or the general scope of the systematic literature review are eliminated in order to preserve the significance and consistency of the overview. On the other hand, every paper that met the requirements of the study objective was included.

2.3 STUDY SELECTION

The study incorporated a rigorous selection procedure that involved two iterations of comprehensive searching. In the first stage of the analysis, the abstracts and titles of articles were reviewed in order to exclude publications that were either irrelevant or duplicates. Following this, all of the texts of the remaining papers were examined in the initial round of screening, eliminating papers that did not satisfy the predetermined criteria (as illustrated in Figure 2). Following the elimination of duplicate articles, any articles that were not relevant to RTs or were written in languages other than English were deemed ineligible. Next, the articles that were chosen from multiple sources were organised and consolidated into an EXCEL® file for convenient access. The articles were diligently examined by four authors, who meticulously identified significant points and offered insightful commentary throughout the ongoing process of revision and taxonomy. The textual content was revised by incorporating the previously made highlights and annotations. The researchers summarised, tallied, and provided explanations for the noteworthy findings. Furthermore, pertinent details were stored in Word and Excel files, including the compilation of surveyed articles, their respective sources, summary and explanation tables, research objectives, review sources, employed datasets, assessment criteria, validation methodologies, and other visual representations. The inclusion of this information in the appendices serves the purpose of providing readers with a comprehensive contextual framework for better comprehending the findings.

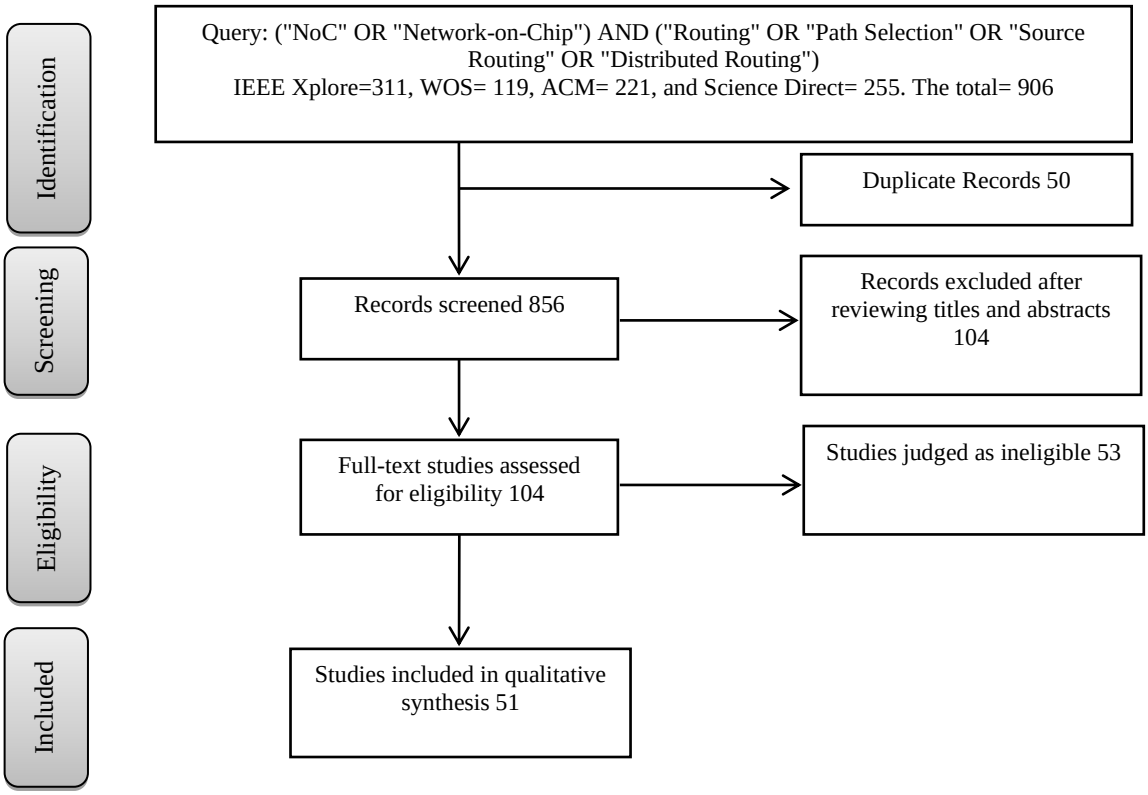

Figure 2. Search query

During a period of 17 years, specifically from 2004 to 2023, a comprehensive search was conducted, resulting in the identification of a total of 906 articles. Following the elimination of redundant occurrences and duplicates and comprehensive evaluation of titles and abstracts, the total count of papers was reduced to 104 articles. After conducting a comprehensive examination of the complete texts, a total of 51 papers were subsequently eliminated, leading to a final compilation of 51 publications. The chosen papers underwent a rigorous review process, serving as a foundation for future research in this dynamic field.

3. RTs NOC- BASED MPSOC: TAXONOMY

The taxonomy employed for monitoring the studies is depicted in Figure 3. This taxonomy accurately depicted the comprehensive development of diverse applications and research endeavours. The findings demonstrated three noteworthy categories. The first category included Congestion Control, the second one was related to Workload Distribution, and finally, Fault Tolerance.

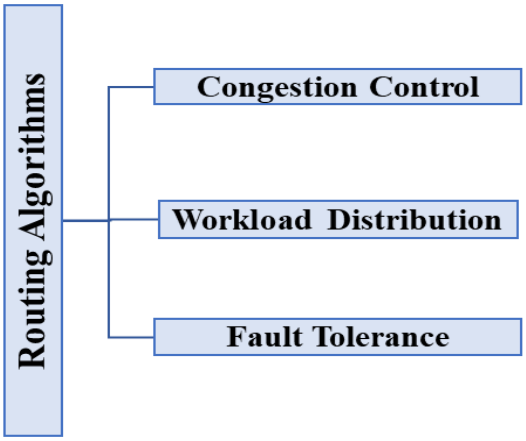

Figure 3. The taxonomy of routing techniques in network-on-chip

3.1. CONGESTION CONTROL

Congestion control is among the critical components of the routing algorithm in NoC-based MPSoC designs. It deals with the methods used in managing and easing network congestion within NoC. As the demand for network resources increases, their supply decreases, and congestion occurs; this results in poor network performance along with high latency and loss of packets.

In [44], the authors consider improving performance and reducing power dissipation in NoC systems by implementing a congestion-sensitive routing algorithm. The main challenge is in the identification of appropriate congestion parameters and direct acquisition data on congestion. The main focus of the literature review was on reliability in NoC systems, but it was mainly related to router ageing effects and how they impact the overall lifespan of a NoC. In [45], this study presented a methodology of modelling where lifetime budgets are given to routers and suggestions were made for routing packets via the paths that had the highest lifetime budget so as to improve both the longevity and reliability of the network. The review suggested that future studies should be directed towards assessing the possible advantages of integrating machine learning methods to help improve the efficiency and longevity of NoC systems. The algorithm tries to achieve adaptive routing in combination with deadlock-free and livelock-free routing. Additionally, a new architecture of routers is designed to be able to handle the given routing algorithm [46]. The results show that DyXY routing is superior to both static XY routing and odd-even routing with respect to different performance metrics. In [47], the study introduced NoC as a possible approach to overcome the shortcomings of on-chip interconnects within Systemon Chip designs. The authors in [48] developed a model for an innovative router architecture that combines adaptive routing techniques in order to improve performance and energy efficiency while ensuring that latency is kept to a minimum.

In [49] the authors studied NOCs in CMP architectures and SoCs, where they particularly pointed out the advantages of adaptive routing compared to oblivious routing algorithms. While adaptive routing has a number of positive features, such as better fault tolerance and increased network throughput plus decreased latency swap, one should take this particular aspect into account since the local decision process during which it happens controls the route's choice globally. To tackle this matter, they suggested the implementation of a technique known as Regional Congestion Awareness (RCA), which aims to enhance the overall equilibrium of the global network. In addition, this article [50] examined the constraints of current locally and globally adaptive routing algorithms within the framework of many-core architectures, wherein multiple applications are executed simultaneously. This statement emphasizes the concerns associated with workload consolidation and the detrimental effects on performance resulting from inadequate network congestion avoidance and interference between applications. In order to tackle these challenges, the paper introduced the concept of Destination-Based Adaptive Routing (DBAR). The authors [51] propose a methodology that incorporates both local and non-local network data to ascertain the most efficient route for packet forwarding. This paper [52] also introduced the Network Information Region framework for the NoC systems. This framework facilitates the examination and incorporation of various combinations of network information and their corresponding routing algorithms. Introduces a novel routing framework called Ant Colony Optimization-based pheromone diffusion within the context of Near-Infrared networks. This framework facilitates the exchange of spatial and temporal network information between neighbouring routers through the process of pheromone diffusion. As the level of intricacy within the network escalates, the occurrence of routing problems hinders optimal performance. The utilisation of ant colony optimisation (ACO) in wide area networks for the purposes of adaptive routing and load balancing is a prevalent technique. Its application in the context of NoC performance enhancement holds promise. Nevertheless, the utilisation of ACO in an NoC systems results in significant implementation expenses.

This research [52] presented a novel routing algorithm termed Adaptive Look Ahead, which integrates the principles of fully adaptive and partial adaptive routing. By determining the subsequent two hops within a node, the algorithm facilitates efficient packet transfer in the following node and only periodically computes the shortest path for packet routing. Another article [53] has proposed an approach called ACO-based Cascaded Adaptive Routing (ACO-CAR). The ACO-CAR algorithm integrates two key components: the optimisation of the routing table to remove superfluous data pertaining to remote destinations and the dynamic exploration of interconnected nodes to enhance the precision of network information retrieval. The authors [54] have emphasised the constraints associated with adaptive routing algorithms in interconnection networks, particularly the adverse impact on global load balance caused by self-interested local decisions. The congestion control scheme under consideration incorporates dynamic input arbitration and adaptive routing path selection strategies in order to achieve a balanced distribution of global traffic load and mitigate congestion resulting from high network utilisation. In certain cases, the accuracy of routing decisions can be compromised because qualitative congestion information may not accurately represent the true state of network congestion. Researchers have suggested a potential solution known as Quantitative Congestion Awareness (QCA) to address this issue [55]. This method aims to mitigate the problem at hand. QCA method collects quantitative congestion data from sources that are not internal to the station by sending percentage differences of desired metrics rather than actual values.

Authors of [56] proposed Global Congestion Awareness (GCA), a novel adaptive routing algorithm for on-chip routers in NoCs. GCA addresses this challenge by leveraging global link state and congestion information to make routing

decisions. Unlike previous techniques that rely on local or regionally aggregated data, GCA utilizes a simple and low-complexity route calculation unit. This approach eliminates myopia in decision-making and prevents the aggregation of unrelated status information. The proposed algorithm offers potential benefits for future CMP designs, improving load balance and reducing wasted power and energy caused by increased latencies. The present investigation [57] aimed to highlight a constraint observed in current adaptive routing algorithms, which fail to consider the presence of virtual channels (VCs) and their occupancy. This oversight results in the propagation of congestion throughout all VCs. To address this constraint, the Footprint routing algorithm is proposed as a potential solution. The subject matter of the aforementioned paper [58] pertained to the hardware realisation of a NoC adaptive routing scheme based on fuzzy logic. This statement underscores the significance of taking into account the dynamic traffic load and power consumption when determining the output port for an incoming flit in NoC systems. In situations where there is a high volume of communication, central routers may experience contention and congestion, leading to elevated levels of latency and power consumption. To tackle these challenges, the concept of a Three-Dimensional Network-on-Chip has been put forth as a potential remedy to enhance the overall performance in terms of throughput, latency, and energy efficiency [59]. This paper [60] presented a novel NoC SerDes transceiver architecture specifically developed for facilitating long-distance interconnectivity within MPSoCs. The transceiver possesses the capability to be smoothly incorporated into heterogeneous MPSoC NoCs as a black box point-to-point connection, thereby facilitating the realisation of a compact top-level floorplan and enhancing energy efficiency. The paper [61] presented two iterations of a novel, dependable, and completely adaptable congestion-aware routing algorithm designed for NoC systems. The newly proposed scheme integrates both local and non-local information when determining the optimal path, effectively achieving a harmonious equilibrium between local and global awareness.
The study [62] introduced a set of cost-effective adaptive routing techniques that leverage specialised channels constructed using Transmission Line technology for the purpose of transmitting long-distance packets. This study presents two novel router architectures, namely SBTR and e-SBTR, which aim to mitigate packet latency by minimising the number of intermediate hops. The present study [63] focused on tackling this particular obstacle by introducing an innovative spiking neural network (SSN) methodology for the prediction of congestion. Future research endeavours may involve investigating the practical implementation of the suggested approach for congestion prediction based on SSN within real-world NoC systems.

It would also be helpful to evaluate the performance of this approach for various traffic cases and network setups. This paper [64] provided a routing algorithm that does not have constraints on the virtual channel and is aware of traffic patterns. The algorithm is a mixed of West-first routing and North-last routing techniques. A hotspot node, along with the mechanism for detecting patterns of a hotspot, is proposed in order to enhance the performance of NoC when traffic variations occur. In [65], this study discusses the problems associated with traditional NoC architectures, such as fast core communication latency and high power consumption in long-distance connections. In order to address the issue of congestion and make a more equitable distribution of traffic between wired and wireless networks, this study suggests using a load-balanced time-based routing algorithm based on congestion awareness. The LTCA protocol provides deathlock-free routing by putting constraints on the packet usage of wireless channels. In the present study [66], an innovative congestion prediction model using SNNs was proposed. The congestion parameter used in the proposed model was input buffer utilisation, which helped to relieve the possible impacts of congestion. The proposed study presents two models – the router and network-level ones, whose purpose is to create precise congestion forecasts for individual nodes of a NoC architecture. The study [67] provided a congestion-aware routing algorithm that shows its effectiveness and low overhead. The algorithm selects a route for the packet based on various factors such as betweenness centrality, historical record of previous packet routes and adaptivity to it. The packet endeavours to maximise its distance along the designated route, but in the event of severe congestion, it possesses the ability to alter its trajectory a finite number of times using the same set of parameters.
This paper [68] presented a novel adaptive routing scheme for NoC systems. The main goal of this plan is to improve the network's performance by providing routers with precise and timely congestion data. The proposed scheme intends to solve the problems typical for current adaptive routing schemes – either they do not have sufficient information about the network, or the data is outdated. In [69], the authors focused on the issue of congestion in communication within chips. This has been identified as one major cause for performance degradation due to data packet stalls and increased latency. A new routing algorithm for NoCs presented in the study uses weighted, minimal, fully adaptive congestion-aware techniques. In [70], this study proposed a new congestion metric for NoCs using betweenness centrality and incorporating network heterogeneity. This solution has significantly reduced average latency and power consumption during its implementation, making it a promising approach to effectively handle congestion on networks of considerable scale present within chips. In [71], this study introduced the ScRN algorithm as a new routing approach for NoCs. There is an appreciable improvement in performance metrics like delay time, throughput and energy utilization when the traffic's geographical location and the system's current state are considered. The simulation results provide empirical evidence supporting the proposed approach's superiority compared to existing solutions. Table 2 shows the summary of studies of Congestion Control.

Table 2. Congestion Control in RTs

Ref	NoC RT	Principle	NoC Status of Congestion	NoC Deadlock Strategy	Advantages	Limitations
[44]	CACBR	Cluster-Based	SN	VC	Congestion-aware, which helps in avoiding congested paths.	Incur additional overhead in maintaining Congestion information.
[45]	NOP	XY	DW	RR	Simple and easy to implement.	Lead to increased latency in certain scenarios.
[46]	DyXY	XY	DW	VC	Adapts to changing network conditions dynamically.	Increased complexity in decision-making.
[48]	Low-Latency Routing	Traffic Monitoring	SN	VC	Minimizes latency for improved performance.	Not perform optimally under high network loads.
[50]	DBAR	RCA 1 D	SN	VC	Adapts routing based on destination characteristics.	Require additional information about destinations.
[51]	CATRA	RCA Quadrant	SN	-	Considers congestion in the trapezoid region.	Complexity may increase in large-scale networks.
[72]	ACO-Phd	ACC	SN	-	Inspired by Ant Colony Optimization for adaptability.	Require tuning for optimal performance.
[52]	ALA	look Ahead	SN	-	Uses look-ahead information for adaptive routing.	Increased complexity due to look-ahead prediction.
[53]	ACO-CAR	ACO	SN	VC	Adapts routing based on cascaded ACO principles.	Require fine-tuning and optimization.
[54]	Congestion-Aware- and-Adaptive	Segmentation	SN	VC	Combines congestion awareness and adaptability.	Increased complexity in decision-making.
[55]	QCA	DRAR	SN	VC	Quantitative congestion awareness for precise routing.	Require additional hardware support for accuracy.
[49]	Adaptive RCA	RCA	SN	VC	Adapts routing based on regional congestion.	Complexity may increase with a large number of regions.
[57]	Footprint	Head of Line	SN	VC	Considers the footprint of the network for routing.	Limitations in scalability.
[58]	FLR	Fuzzy Logic	SN + TB	VC	Load-balanced time-based congestion-aware routing.	Increased latency under certain conditions.
[59]	MiCRA	-	SN	VC	Uses hierarchical clustering for efficient routing.	Require specific network configurations for effectiveness.
[60]	AC DC	Dropping packet	SN	VC	Adaptive and considers congestion for routing decisions.	Require tuning for optimal performance.
[61]	FACARS	RCA and DBAR	SN	VC	Fully adaptive to congestion for improved performance.	Increased complexity may affect scalability.
[62]	SB IR and e-SBTR	Back Pressure	SN	RR	Uses spiking neural networks for routing decisions.	Require specialized hardware support.
[63]	Exploring SNN	SNN	SN	VC	Explores spiking neural networks for adaptive routing.	Complexity may increase with the use of SNN.
[64]	Hotspot-Patten-Aware	West-first and North-Last	SN	RR	Takes into account hotspot patterns for routing.	Require accurate hotspot prediction for effectiveness.

[65]	LTCA	Wireless Routing	-	RR	Balances load based on time and congestion.	Increased complexity in implementation.
[66]	SRM	SNN 1	SN	VC	Utilizes a spike-response model for routing decisions.	Require specialized hardware support.
[67]	Novel Congestion Aware Routing	Packet History	SN	VC	Offers a novel approach to congestion-aware routing.	Effectiveness may depend on specific network scenarios.
[68]	URCA	DBAR	SN	VC	Unbiased regional congestion awareness for routing.	Require accurate estimation of regional congestion.
[69]	DyXYYX	RCA and DBAR	SN	VC	Dynamically adapts routing based on XY and YX dimensions.	Increased complexity in decision-making.
[51]	Congestion Aware Routing	CATRA	SN	VC	Basic congestion-aware routing for improved efficiency.	Not handle dynamic network conditions optimally.
[70]	Heterogeneous Congestion Criterion	Novel Congestion Aware Routing	SN	VC	Considers heterogeneous congestion for adaptive routing.	Additional information may be required for accurate decisions.
[71]	ScRN	RCA and NOP	SN	VC	Hybrid approach for regional congestion awareness.	Increased complexity due to the combination of approaches.
[56]	GCA	Global Congestion Awareness	SN	VC	Considers global congestion for adaptive routing.	Require a comprehensive view of the entire network.

*
- NoC Status of Congestion: Logic Based LB, Side Network: SN, Table Based: TB, Dedicated wire: DW
- NoC Deadlock Strategy: Router Restriction: RR, Virtual Channel: VC, Hop count Priority: HCP, Heuristic Tree: HT.

3.2. WORKLOAD DISTRIBUTION

Workload distribution is an important aspect of routing algorithms in the NoC-based MPSoC architectures. It involves the efficient distribution of communication traffic and computational tasks across the network to achieve load balancing and optimize system performance.

The research [73] concluded by outlining an adaptive two-way routing technique for hotspots in NoC multiprocessors. The algorithm improves upon conventional routing techniques by lowering packet latency by detecting hotspots and implementing route limitations. The experimental analysis proves that the proposed technique is effective in reducing congestion even when dealing with hotspot cores. Reference [74] developed a routing algorithm for NoC architectures. The algorithm aims to efficiently distribute on-chip traffic across the network by using global traffic information rather than relying solely on local congestion information. It accomplishes this by employing a lightweight and efficient control network that monitors on-chip traffic and collects the necessary global information to determine appropriate paths between communicating nodes. The proposed method is demonstrated to outperform conventional deterministic and adaptive routing mechanisms in terms of congestion avoidance and load balancing based on experiments conducted on a 7x7 NoC using several benchmarks. The paper [75] introduced an innovative methodology to tackle the problem of adaptiveness in NoC routing. The proposed approach enhances network performance by introducing additional routing options and distributing traffic load in non-congested regions through the inclusion of cycles in the channel dependency graph, subject to specific constraints. This paper [76] emphasized the importance of addressing system-level reliability concerns within the emerging NoC paradigm for MP-SoCs. The proposal suggested the integration of adaptiveness into data communication systems in order to enhance their ability to withstand manufacturing faults. This paper emphasized the importance of a comprehensive study on tradeoffs in performance and cost related to adaptive routing schemes used with NoC fabrics, considering application-specific requirements.

In addition, the research [77] introduced a new routing method named Nue that is not reliant on network topology. Nue addresses the problems of obtaining efficient and deadlock-free routing in lossless interconnection networks. Nue manages to avoid deadlocks while calculating the path in a way that optimizes load balancing within previously set virtual channel limits. The approach was demonstrated with the use of InfiniBand architecture. Another article [78] presented a proposal for redirecting routing in hierarchical mesh NoCs and introduced interleaving techniques along with shifting techniques to improve the power efficiency and performance of the implementation. Evaluated results confirm that these techniques reduce power dissipation and improve network performance, thus making them important parameters in designing low-cost NoC implementations. Further, the authors [79] sought to provide profound insights

into how NoC parameters impact performance in MPSoC architectures. This research will improve the understanding of how different NoC design decisions affect application execution in MPSoCs. In [80], a partially adaptive routing algorithm was presented for mesh network-on-chip architectures. The utilization of the algorithm effectively diminishes the necessity for virtual channels while maintaining optimal performance. This proposed algorithm presents a potentially promising approach to reduce complexity and power consumption in MNoCs, all while ensuring sustained levels of performance.

In an extensive study [81], , researchers introduced MWPF (Multiple Whole Packet Forwarding), an advanced routing algorithm specifically designed for NoC systems. The MWPF algorithm is uniquely tailored to tackle the specific challenges faced by NoCs and exhibits remarkable enhancements in latency, throughput, and maximum latency reduction compared to existing methodologies. Consequently, it showcases exceptional capabilities when implemented within NoC architectures. Additionally, another significant contribution presented in this research [82] focuses on Sora: an innovative software radio platform meticulously crafted for commodity PC architectures. By skillfully merging hardware and software-defined radio (SDR) platforms' strengths together, Sora overcomes intrinsic obstacles associated with achieving high-speed SDR performance on PC architectures. Its versatility has been successfully demonstrated across various wireless system developments, including 802.11 and LTE domains—proving its effectiveness transcends different applications. In a different study [83], researchers proposed the Traffic Allocation routing algorithm as a viable solution to address the challenges faced in developing efficient routing algorithms for the NoC architectures. This innovative algorithm integrates traffic allocation registers and leverages local computations to evaluate traffic loads, resulting in improved performance when compared with existing algorithms. Through extensive simulations, empirical data that unequivocally supports the efficacy of this novel approach was obtained, highlighting its ability to enhance the overall performance of NoC architectures. This research paper [84] delivered a conceptual framework for the development of, in part, adaptive common sense-based totally allotted routing algorithms, with a selected emphasis on the Lattice-based total Turn Model. The model that has been proposed presents a comprehensive framework, and the accompanying theorems offer treasured insights for the development of lattice-primarily based routing algorithms that are loose from deadlock. The LBRA algorithm, while applied in line with this model, reveals notable upgrades in overall performance as compared to current methodologies when comparing exclusive site visitor patterns.

This study [85] introduced LAXY routing algorithm as a mitigation approach for the limited lifetime issue of NoC architectures, which is due to ageing processes. LAXY improves the lifespan of routers and interconnects as well as reduces packet latency by effectively spreading out packets in the network. The proposed approach has demonstrated promising results in simulations and presents considerable improvements to the average time until failure and overall packet latency with only marginally higher area overheads. Furthermore, the article [86] also presented and analyzed the design of Repetitive Turn Model (RTM) logic-based routing algorithms for two-dimensional mesh-based NoCs. The design of RTM algorithms relies on the identification of routing algorithms, which are characterized by prohibited turns that repeat and lower rout pressures. The given simulation results show significant betterment in performance relative to the customary version of Odd-Even routing algorithm. The research [87] proved ESPADA to be a feasible approach for constructing effective routing algorithms in NoCs. ESPADA provides increased fault tolerance and superior performance with the use of virtual channels for throughput improvement as well as deadlock avoidance. Another researcher [88] suggests a new deterministic routing algorithm called ZigZag routing algorithm to solve the problems of current ones. The ZigZag algorithm compares the distances in X and Y directions, sending packets towards directions with more distance until these bottoms are equal. In [89], a variation of fault-tolerant routing algorithms was presented for NoC systems. This algorithm is based on the XY algorithm and seeks to increase system performance, but it does not use virtual channels. Hence, it shows significant prospects in terms of space allocation and power saving. Verification of the algorithm's effectiveness was carried out in three stages, through simulation and FPGA-based validation methods, providing evidence that this design is reliable and feasible considering its outstanding performance within NoC systems. Furthermore, this article [90] suggested a new technique called EOmesh that could nearly achieve optimal bandwidth allocation in NoC-based manycore systems specifically designed for CRTESs. Through the combination of a predictable routing strategy with weight allocations, EOmesh obtains improved average system performance in addition to minimizing worst-case execution time outcomes possible when compared against existing weighted mesh configurations. Thus it provides a useful way to improve efficiency and reliability in CRTESs by overcoming mismatches typical for such architectures.

Researchers [91], introduced a novel algorithm called workload-aware routing WAR For CMPs in NoC architectures Assistant. This novel approach is intended to balance the network traffic and extend the system’s life span using workload signatures; priority-based routing techniques are also implemented. Another study found that this algorithm helps in the redistribution of traffic, which enhances the system's performance level and reduces congestion at the central. The encircle routing algorithm was presented in another article [92]. This algorithm, by the redistribution of traffic, helps enhance system performance and reduce congestion at the centre hub of the network. Lastly, another research paper [93] provided an extensive analysis and comparative evaluation of two prominent routing algorithms - XY Routing and Odd-even Routing - within a 3x3 mesh topology NoC. The study encompassed thorough examinations and simulation-based comparisons to assess their respective merits. Additionally, Table 3 offers a concise summary that outlines key findings from studies related to Workload Distribution.

Table 3. Workload Distribution in RTs

Ref	NoC RT	Principle	NoC Deadlock Strategy	Advantages	Limitations
[73]	Two Way Odd-Even	Odd-Even	TR	Simple and easy to implement.	Not optimal for all network topologies.
[74]	Load-Balanced-Link- Distribution	Link Distribution	VC	Balances load across links for improved performance.	Additional information about link states may be required.
[75]	CHARM	Turn Model	VC	Congestion-aware and highly adaptive to dynamic conditions.	Increased complexity may impact scalability.
[76]	Adaptive Routing	Pressure Model	TR	Dynamically adapts to changing network conditions.	Incur additional overhead during decision-making.
[77]	Nue	Dependency Graph	TR	Provides a unique approach to adaptive routing.	Effectiveness may depend on specific network scenarios.
[78]	HDR	Deflection Routing	D	Uses hierarchical mesh structures for efficient routing.	Complexity may increase in large-scale hierarchical networks.
[79]	PW-Odd-Even	Odd-Even	TR	Implements a parallel odd-even routing scheme.	Not optimal under certain traffic patterns.
[80]	PEPAR	-	TR	Optimized for power efficiency.	Sacrifice some adaptability for power savings.
[81]	MWPF	Whole Packet Forwarding	VC	Utilizes multiple packet forwarding for increased throughput.	Increased hardware complexity may be required.
[82]	SoRA	Network Pressure	TR	Unique approach to routing decisions.	Limitations in scalability and generalizability.
[83]	TA	-	-	Efficiently allocates traffic for improved performance.	Require accurate traffic prediction for effectiveness.
[84]	LBRA	Turn Model	TR	Utilizes a lattice structure for routing decisions.	Limitations in adapting to dynamic conditions.
[85]	LAXY	Turn Model	TR	Considers location-based aging-resilient routing.	Increased complexity due to the aging-resilient mechanism.
[86]	RTM	Turn Model	TR	It uses a repetitive turn model for routing decisions.	Not optimal under certain traffic patterns.
[87]	Mini-ESPADA	ESPADA	VC	Implements dynamic channel acquisition for efficient routing.	Complexity may increase due to dynamic channel management.
[88]	ZigZag	XY	VC	Unique routing approach using zigzag patterns.	Not be optimal for all network topologies.
[89]	Modified XY	XY	VC	A modification of the XY routing scheme.	Effectiveness may depend on the nature of the modification.
[90]	EOmesh	XY	VC	Utilizes even/odd mesh for routing decisions.	Limitations in adapting to dynamic conditions.
[91]	WAR	Workload Signature	VC	Adapts routing based on workload conditions.	Require accurate workload prediction for effectiveness.
[92]	Encircle	XY	TR	Implements an encircling strategy for routing.	Not optimal under certain network topologies.
[93]	Odd-Even	Turn Model	TR	Simple and easy to implement.	Not optimal for all network topologies.

*
- NoC Status of Congestion: Logic Based LB, Side Network: SN, Table Based: TB.
- NoC Deadlock Strategy: Router Restriction: RR, Turn Restriction: TR, Deflection: D, Virtual Channel: VC, Hop count Priority: HCP, Heuristic Tree: HT.

3.3. FAULT TOLERANCE

The issue of fault tolerance is very critical in the design of NoC-based MPSoC architecture routing algorithms. It is the capability of a system to keep working efficiently despite such faults or failures represented by link failover, router fails and so on. In [93], the study described TRACK, a fast and scalable routing reconfiguration algorithm for network-on-chip architectures. TRACK improves performance, lowers latency and increases throughput because it uses logic-based routing that reconfigures only those nodes affected. The algorithm furthermore shows possible reductions in hardware expenses, making it a promising solution for avoiding failures in NoC designs. Furthermore, the research provided [94] CURE a new NoC design framework that uses deep reinforcement learning approaches. The proposed solution is thought to help accomplish several goals, which are decreasing network latency, increasing energy efficiency, and improving fault tolerance for both transient errors and permanent defects. The simulation results using the PARSEC benchmark prove that CURE is efficient. The experimental findings show a splendid reduction in end-to-end latency packet by 39%, great enhancement of energy efficiency from, and a decrease in static as well dynamic power consumption with per cent. In addition, the authors [95] investigated challenges faced by NoC systems caused by congestion, faults and process variants, all of which have negative impacts on system performance.
The experimental results demonstrate a significant reduction in end-to-end packet latency by 39%, a notable improvement in energy efficiency by 92%, and a decrease in static and dynamic power consumption by 24% and 38%, respectively, compared to conventional solutions. Moreover, the authors [96] analysed the difficulties encountered by NoC systems as a result of congestion, faults, and process variation, all of which can have detrimental effects on system performance. The aforementioned concerns in asynchronous NoCs necessitate the implementation of an adaptive routing algorithm that is congestion-aware, fault-tolerant, and process variation-aware. The CFPA routing algorithm, as suggested, is assessed in comparison to other widely used routing algorithms across various NoC topologies and dimensions. Furthermore, this study [97] developed a novel routing and addressing design named Hierarchical Routing Architecture (HRA), which overcomes the current Internet's scalability concerns. The report discusses ongoing research work in the IETF and IRTF Routing Research Group (RRG) to investigate new routing scalability options. This paper [98] aimed to explore the intricate task of developing interconnection networks that are both scalable and reliable for multicore chips. The primary focus of this investigation centres on the issue of optimising routing efficiency. The proposed solution, known as logic-based distributed routing (LBDR), seeks to address the limitations of routing tables, which can potentially lead to scalability challenges in terms of latency and area. In contrast, the LBDR mechanism presents a novel circuit design that enables the computation of a group of three bits for each switch output port. This design effectively replicates the functionality of routing algorithms that are typically implemented using routing tables. Finally, this paper [99] expressed an adaptive multi-path routing (AMP) algorithm that has been specifically developed to address the requirements of dynamic traffic engineering in autonomous systems. In contrast to current multi-path routing methodologies, the AMP framework prioritises utilizing local information at individual nodes instead of maintaining a comprehensive understanding of the entire network. The objective of AMP is to decrease signalling overhead and memory consumption in routers by restricting the accessible information to a localised scope. Table 4 shows the summary of studies on Fault Tolerance.

Table 4. Fault Tolerance in RTs

Ref	NoC RT	Principle	NoC Status of Congestion	NoC Deadlock Strategy	Advantages	Limitations
[94]	TRACK	D^2 LBDR	LB	RR	Simplified and easy to implement.	Lack of sophistication for complex network topologies.
[95]	CURE	Deep reinforcement learning	SN	VC	Congestion-aware and fault-tolerant.	Increased complexity due to fault tolerance.
[96]	CFPA	Process Variation	SN	HCP	Adapts to congestion, faults, and process variations.	Increased complexity may impact scalability.
[97]	HRA	A-Star Search	SN	HT	Utilizes a hierarchical structure for	Complexity may increase in large-scale hierarchical

					efficient routing.	networks.
[98]	LBDR	LBDR	TB	VC	Distributed routing based on logical considerations.	May have limitations in adapting to dynamic conditions.
[99]	Adaptive Multi-path Routing	DyAD	SN	-	Utilizes multiple paths for improved performance.	Increased complexity and resource usage due to multiple paths.

*

- NoC Status of Congestion: Logic Based LB, Side Network: SN, Table Based: TB.
- NoC Deadlock Strategy: Router Restriction: RR, Virtual Channel: VC, Hop count Priority: HCP, Heuristic Tree: HT.

4. COMPREHENSIVE SCIENCE MAPPING ANALYSIS

Increased contributions and performed studies involve the problematic undertaking of obtaining critical evidence from existing literature. Preserving this literature is an essential duty due to the great dissemination of each practical and theoretical contribution. Many students endorse employing systematic critiques and meta-evaluation as techniques to organize previous findings, summarize troubles, and identify study gaps. Systematic evaluations make a contribution to increasing the know-how base, refining research design, and synthesizing literature effects. Nevertheless, these evaluations face demanding situations associated with reliability and objectivity as they depend upon the authors' views in restructuring previous literature findings. To enhance transparency in summarizing these findings, various works propose a complete review of the routing techniques utilising R-device and VOSviewer [24]. The bibliometrics method, recognized for supplying conclusive outcomes, exploring study gaps, and concluding literature findings with excessive reliability and transparency, is recommended. Moreover, those tools are handy as open-supply sources, requiring no advanced skills. Consequently, this looks at embracing the bibliometric technique, which is unique in the subsequent sections.

4.1. CLOUD OF WORDS

Figure 5 displays a word cloud that showcases the prevailing and noteworthy terms extracted from prior research, providing a succinct summary and restructuring of the data.

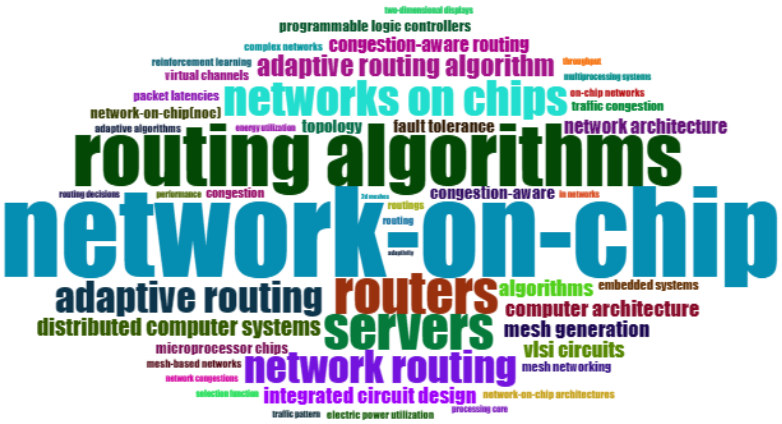

Figure 4. Word cloud

The relative size of the keywords depicted in Figure 4 corresponds to their respective frequencies of occurrence within the body of research literature. The presence of larger keywords signifies a higher frequency of occurrence, whereas thinner terms indicate a lower frequency of appearance within the existing body of literature. Network-on-chip, routing algorithms, and network routing are identified as significant areas of study. Moreover, the existing body of literature extensively examines the application of machine learning algorithms in supporting designers. Nevertheless, the literature highlights the significance of assessing and prioritising factors in performance routing algorithms in the context of MPSoC.

4.2. CO-OCCURRENCE

Co-occurrence networks are established by utilising the prevalent terms that have been identified in prior scholarly investigations. The analysis of co-occurrence serves as a means to examine the network structure, which can provide

valuable insights into the theoretical framework that underlies a particular research domain. These insights offer advantages not only to professionals, policymakers, and academics within the respective discipline but also for enhancing comprehension of the interconnections among terms and concepts. Figure 5 presents co-occurrence networks, which facilitate the understanding of commonly utilised terms and their interconnections within the field of research.

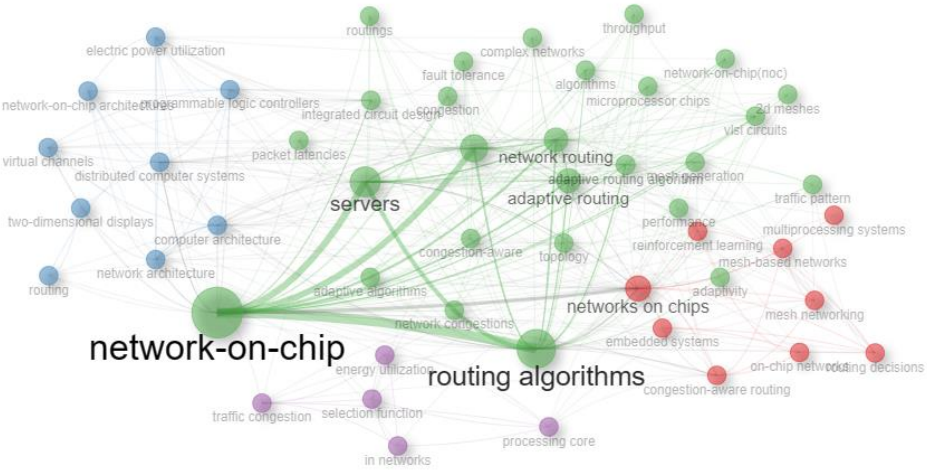

Figure 5. Co-Occurrence

The co-occurrence network serves as a visual representation of the interconnections among subjects identified in the existing body of literature. The structure is composed of interconnected lines and nodes, wherein the larger nodes symbolise the prevailing concepts found in the literature. Policymakers and researchers have the opportunity to utilise these network structures in order to facilitate the reorganisation of existing information and research findings. Within the domain of MPSoC, the concepts of network-on-chip and routing algorithms have emerged as prominent terminologies that have been extensively employed by prior researchers, thereby underscoring their notable importance within this field.

4.3. MOST HIGHLIGHTED ARTICLES

To enhance comprehension of the advancements in this field, it is imperative to discern the seminal works that have exerted a substantial influence on the scholarly discourse. Moreover, an examination of citation patterns within the existing body of literature can provide valuable insights regarding the prospective trajectory of the discipline. Table 5 presents a comprehensive overview of the five most influential papers that have significantly contributed to the field. These scholarly articles have made significant contributions to the field, both in terms of theoretical advancements and practical applications. Frequently, individuals in academic discourse tend to introduce a theoretical quandary and subsequently propose resolutions within their scholarly contributions. Table 5 functions as a valuable tool that showcases the pivotal studies in the respective field, elucidating their significance and influence within the existing body of scholarly work.

Table 5. Most important studies

DOI	TC	TCpY
10.1109/ASAP.2015.7245728	431	47.89
10.1109/date.2012.6176488	60	5
10.1109/DATE.2008.4484871	60	3.75
10.1109/NESEA.2011.6144949	58	4.462
10.1109/ESTMED.2006.321278	41	2.278

DOI: Digital Object Identifier, TC: total citations, TCpY: The citations rate per year

4.4. THREE-FIELD PLOT

Journals, affiliations, and countries are interconnected and can offer valuable information. Figure 8 illustrates a three-field arrangement that visually represents the interconnected networks among prominent publishing venues (located on the right side), affiliations (located in the centre), and nations (located on the left side). This layout offers significant insights into the dynamic interactions between these entities. The analysis revealed a substantial volume of published articles about routing algorithms, with a noteworthy prevalence of authors hailing from Iran, China, and India. Islamic Azad University and the University of Catania have emerged as prominent academic institutions in routing algorithms in MPSoC. Figure 6 illustrates widespread interest in these techniques across multiple countries globally. The resource

in question proves to be a valuable asset for emerging authors, as it offers a comprehensive survey of the literary field while highlighting potential avenues for additional research and collaborative endeavours.

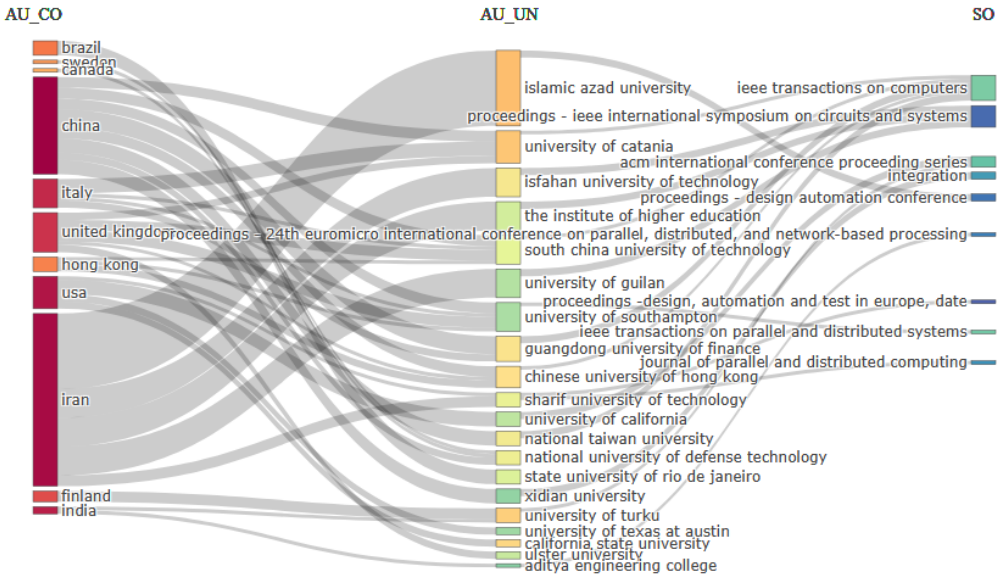

Figure 6. Three-fields plot

5. RECOMMENDATIONS

This section provides a broad direction for future studies and recommendations using the TCCM framework, which can be further discussed in theory, context, characteristics, and methodology [36]. It does so by presenting multiple beneficial aspects of insight and enhancing the impact of existing review-based suggestions. This will assist researchers in the future in finding gaps in every aspect of the TCCM framework, especially in the routing algorithms domain. Figure 7 shows the recommendations.

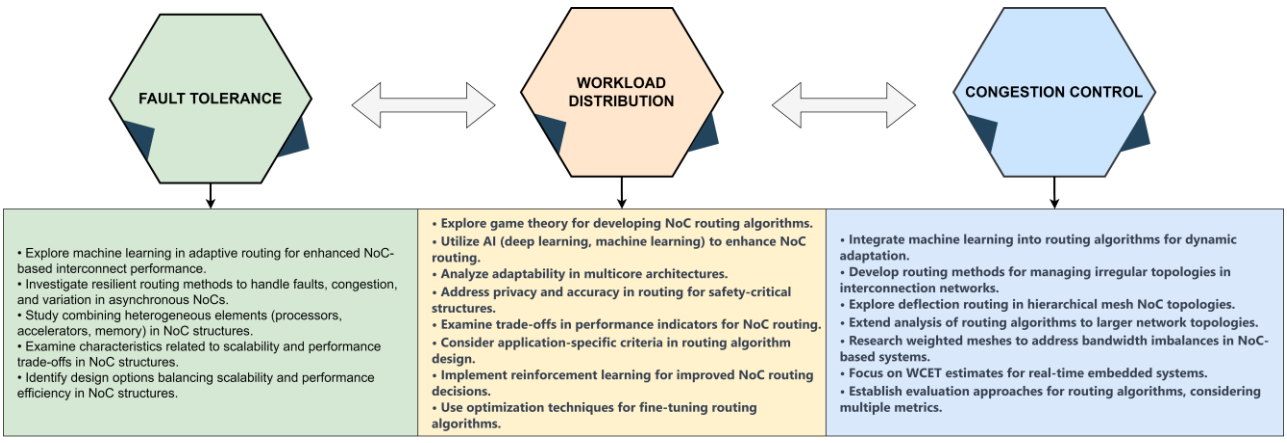

Figure 7. The major recommended aspects of routing techniques of NoC

5.1. CONGESTION CONTROL

In the context of future directions about theory, the investigation of the effectiveness of game theory structures in developing routing algorithms for NoCs and exploring the cooperation of AI approaches, such as deep learning and machine learning, to improve the flexibility and performance of routing algorithms in NoCs are the most significant directions [45], [63]. In terms of context direction, the analyses of the adaptability and flexibility of routing algorithms in the context of heterogeneous multicore architectures and the cooperation of specialised accelerators [60], [70] and considering the effects of privacy and accuracy concerns on the design and application of routing algorithms, especially in NoCs for safety-critical structures are vital context directions [63]. Moreover, characteristics directions can be examine the trade-offs between performance indicators, including latency, throughput, and energy usage, when designing and refining routing algorithms for NoCs [59], [64] and investigating the effect of application-specific criteria on the design and optimisation of routing algorithms [51]. Furthermore, the methodology directions can be investigated based on exploring an opportunity for reinforcement learning algorithms, such as Q-learning or deep Q-

networks, in improving the decision-making process of routing algorithms for NoCs and investigating the implementation of computational optimisation techniques, such as linear programming or evolutionary techniques, to fine-tune routing algorithms and accomplish global optimisation [66].

5.2. WORKLOAD DISTRIBUTION

In the realm of theoretical recommendations for workload distribution, exploring the potential integration of machine learning approaches, such as reinforcement learning or deep learning, into routing algorithms is suggested. This integration enables dynamic adaptation of routing decisions based on real-time circumstances in the network and traffic. Developing new routing methods that can manage irregular topologies caused by design decisions or hardware failures in lossless interconnection networks found in high-performance computing systems, data centres, and network-on-chips [77]. Research deflection routing approaches in hierarchical mesh NoC topologies further, examining other tactics such as interleaving and shifting to reduce the number of high radix crossbars while maintaining network performance. Additionally, extending evaluation and analysis of routing algorithms to larger network topologies beyond 16x16 2D mesh, taking into account the effect of scalability on the effectiveness and performance of routing algorithms and looking into and suggesting new algorithms that overcome the drawbacks of current ones while taking into account load balancing, traffic patterns, and network conditions are the most vital context direction [84]. Furthermore, research using weighted meshes to mitigate the pathological behaviour brought on by significant bandwidth imbalances in NoC-based many-core systems, focusing on precise worst-case execution time (WCET) estimates for crucial real-time embedded systems, is the direction of the most effective characteristic [88]. Moreover, the methodology directions can be establishing comprehensive evaluation approaches for routing algorithms, considering multiple performance metrics, scalability, adaptiveness, and resource utilisation to deliver a holistic agreement of their strengths [90].

5.3. FAULT TOLERANCE

For the third category (fault tolerance), the theory recommendations are to explore the opportunity cooperation of machine learning algorithms in adaptive routing to enhance the performance and effectiveness of NoC-based interconnects [95] and investigate resilient routing methods that can successfully handle faults, congestion, and handle variation in asynchronous NoCs, leading to increased performance and fault tolerance. Besides, the context of future directions can be studied by combining heterogeneous elements, such as processors, accelerators, and memory units, within NoC structures intended for effective and scalable interaction between diverse computing elements. Furthermore, study the characteristics associated with the scalability and performance trade-offs of NoC structures, working to identify design options that can supply a balance between scalability and performance efficiency.
Analyse the characteristics of NoC architectures concerning security and privacy aspects [99].

6. KEY CHALLENGES: CRITICISM AND GAP ANALYSIS

This section explores the complicated landscape of major challenges that are linked to routing techniques based on NoC in MPSoC architectures. As MPSoCs advance to meet the growing requirements of contemporary computing applications, the significance of NoC becomes more crucial in delivering a flexible and effective communication infrastructure. However, the implementation of efficient routing algorithms within this intricate network structure is faced with challenges that go beyond typical limits. The key challenges are linked to the main three categories of routing issues in this study, congestion control, workload distribution, and fault tolerance respectively. Figure 10 shows the key challenges.

6.1. CONGESTION CONTROL

- **Insufficient comparative analysis:** Numerous researchers provide novel routing algorithms or designs without conducting comparisons to established methodologies. It is necessary to do a thorough study in order to comprehend the worth and superiority of the provided solutions, whether in comparison to recognized algorithms or industry standards.
- **Inadequate discussion on limitations:** The majority of the study mostly focuses on the advantages and favourable outcomes of their proposed remedies. However, there is a notable lack of information on potential constraints or unfavourable characteristics and instances when the suggested algorithms might perform poorly. In order to improve awareness of these idiosyncrasies, it is important to obtain a comprehensive overview.
- **Limited elaboration of practical implementation factors:** While studies provide novel solutions, they fail to address practical challenges and concerns that would be crucial for implementing these solutions in real-world scenarios. To enhance the usefulness of research, it is essential to carefully consider hardware restrictions, compatibility with existing systems, and possible implementation challenges.
- **Inadequate evaluation of scalability:** Various studies analyze how different solutions work for the given NoC sizes or topologies. However, a profound scalability analysis is needed particularly for larger and more

complex NoCs. The ability of the proposed solutions to efficiently address increasing network capacities and workloads should be another crucial aspect of the study.

- **Lack of discussion about power consumption:** Although several studies briefly address the performance elements of their recommended solutions, there is a notable absence of discussion about energy efficiency. It is crucial to conduct a comprehensive analysis and documentation of the consequences of the implemented algorithms and architectures on energy use, especially considering the increasing importance of power efficiency issues.

6.2. WORKLOAD DISTRIBUTION

- **Insufficient congestion management:** The main focus of MPSoC is congestion control, particularly in relation to adaptive routing approaches [73]. Throughout this survey, we observed that numerous suggested challenges revolve around achieving a balanced equilibrium between local and global traffic data to make optimal routing decisions.
- **Negligible tradeoff:** The difficulty arises in balancing the tradeoff between the simplicity and effectiveness of routing algorithms for Mesh NoC. During our study, we observed that different routing algorithms frequently need greater complexity, resulting in additional virtual channels and increased power usage. Therefore, we suggest thoroughly examining to provide more efficient alternatives with reduced power consumption.
- **Inadequate coordination between latency and average hop count**: Across our investigation, we observed that the main difficulty is in finding a compromise between latency and average hop count while also obtaining a significant enhancement in network traffic distribution for a long-lasting NoC lifespan.
- **Insufficient optimization**: The task involves optimizing routing algorithms for deep submicron technology, reducing congestion, and enhancing latency in contemporary, intricate MPSoC designs. Furthermore, our investigation revealed a scarcity of papers addressing the drawbacks of optimization.

6.3. FAULT TOLERANCE

- **Lack of enhanced NoC reliability:** The challenge is to enhance NoC reliability by reducing latency, improving throughput, and minimizing hardware costs in the face of single and double-link failures. However, we have not observed studies that studied its effect on design overhead.
- **Less designing scalable:** The problem is creating interconnection networks for multicore devices that are both scalable and dependable, considering aspects like power consumption, area, and ultra-low latencies. Although 2D meshes are commonly used in NoC designs, the increasing occurrence of irregular topologies caused by heterogeneous cores, faults, and failures is rarely discussed.
- **Poor dynamic traffic management**: The task is to develop an algorithm that achieves the ideal balance between efficiency and simplicity for managing traffic in autonomous systems. Unfortunately, most previous studies did not address the emphasis on implementation.
- **Limit in utilizing the MCDM techniques:** Many previous studies dealt with the evaluation of the routing techniques from one aspect, for example, energy consumption, while not considering the entire calibration for evaluation, so we recommend using MCDM techniques.

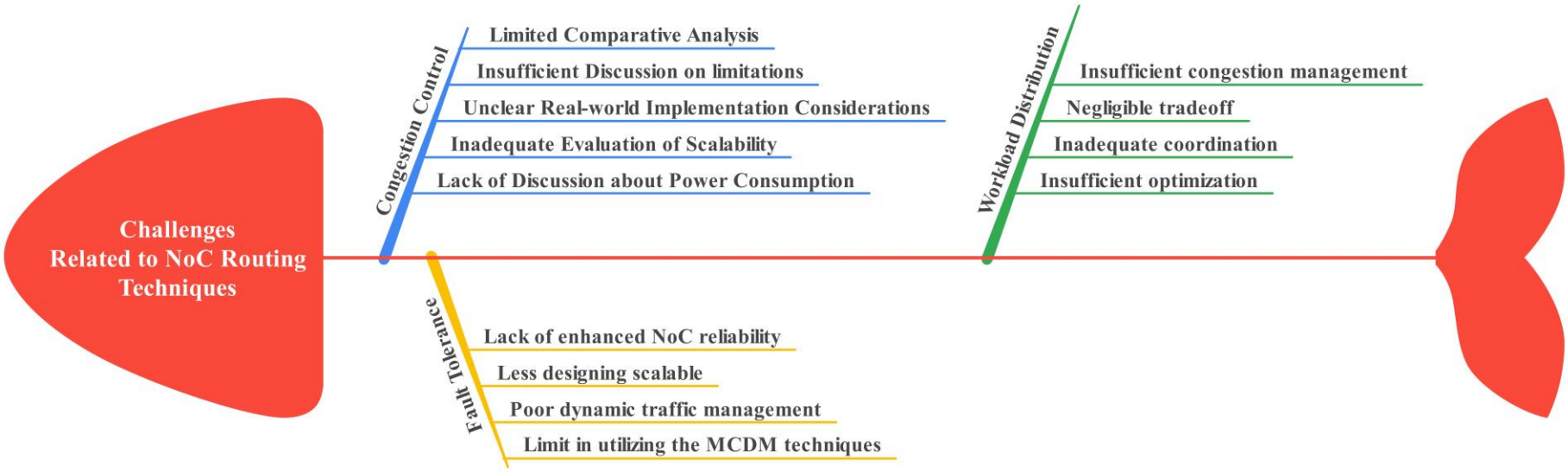

Figure 8. Key challenges

7. CONCLUSION

The quantity of research on RTs in NoC-based MPSoC systems for the IoT domain is steadily growing. However, these investigations have certain specific challenges that have not been addressed. RTs in NoC-based MPSoC are hot topics that require more research. Gaining a profound understanding of this trend subject is crucial. The primary contribution of this paper is an extensive examination and categorization of works about the subject matter.

Additionally, several distinct patterns in the literature have been identified. The collected prior studies are categorized into three groups: Congestion Control, Workload Distribution, and Fault Tolerance. We conducted an in-depth review of several publications to emphasize the challenges and recommendations pertaining to triage RTs in NoC and identified some areas that require additional gaps. Multiple recommendations for managing and monitoring these techniques are offered accordingly. Furthermore, this overview comprehensively analyzes the existing data and evidence. Also, it presents a clear overview of previous research via bibliometric analysis and TCCM, which assists in recognizing sectors where extra investigation is needed. This paper provides valuable insights into the challenges associated with RTs in NoC-based MPSoCs, offering direction to other scholars in addressing routing impediments. The vast majority of these challenges are associated with unclear practical implementation strategies, inadequate assessment of scalability, insufficient management of congestion, power consumption, energy efficiency, minimal tradeoff, utilization of MCDM techniques, limited scalability in design, and inadequate optimization. This systematic review also outlines and establishes an essential source for further studies to develop and enhance the understanding of RTS in the NoC-based MPSoC domain.

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CONFLICTS OF INTEREST

None

REFERENCES

[1] H. Ali et al., “A survey on system level energy optimisation for MPSoCs in IoT and consumer electronics,” Computer Science Review, vol. 41, p. 100416, 2021, doi: 10.1016/j.cosrev.2021.100416.

[2] A. A. J. Al-Hchaimi, N. Bin Sulaiman, M. A. Bin Mustafa, M. N. Bin Mohtar, S. L. B. M. Hassan, and Y. R. Muhsen, “A comprehensive evaluation approach for efficient countermeasure techniques against timing side-channel attack on MPSoC-based IoT using multi-criteria decision-making methods,” Egyptian Informatics Journal, vol. 24, no. 2, pp. 351–364, 2023.

[3] A. A. J. Al-Hchaimi, N. Bin Sulaiman, M. A. Bin Mustafa, M. N. Bin Mohtar, S. L. B. Mohd, and Y. R. Muhsen, “Evaluation Approach for Efficient Countermeasure Techniques Against Denial-of-Service Attack on MPSoC-based IoT Using Multi-Criteria Decision-Making,” IEEE Access, 2022.

[4] S. H. Z. Al-Enzi, S. Abbas, A. A. Abbood, Y. R. Muhsen, A. A. J. Al-Hchaimi, and Z. Almosawi, “Exploring Research Trends of Metaverse: A Bibliometric Analysis BT - Beyond Reality: Navigating the Power of Metaverse and Its Applications,” 2023, pp. 21–34.

[5] Y. R. Muhsen, N. A. Husin, M. B. Zolkepli, N. Manshor, and A. A. J. Al-Hchaimi, “Evaluation of the Routing Algorithms for NoC-Based MPSoC: A Fuzzy Multi-Criteria Decision-Making Approach,” IEEE Access, 2023.

[6] L. Wang, S. Ma, C. Li, W. Chen, and Z. Wang, “A high performance reliable NoC router,” Integration, vol. 58, pp. 583–592, 2017, doi: https://doi.org/10.1016/j.vlsi.2016.10.016.

[7] T. H. Vu, Y. Okuyama, and A. Ben Abdallah, “Comprehensive analytic performance assessment and K-means based multicast routing algorithm and architecture for 3D-NoC of spiking neurons,” ACM Journal on Emerging Technologies in Computing Systems (JETC), vol. 15, no. 4, pp. 1–28, 2019.

[8] R. R. R.S. et al., “DeepNR: An adaptive deep reinforcement learning based NoC routing algorithm,” Microprocessors and Microsystems, vol. 90, p. 104485, 2022, doi: https://doi.org/10.1016/j.micpro.2022.104485.

[9] M. Soni and M. A. Shnan, “Scalable Neural Network Algorithms for High Dimensional Data,” Mesopotamian

Journal of Big Data, vol. 2023, pp. 1–11, 2023.

[10] T. H. Vu, O. M. Ikechukwu, and A. Ben Abdallah, "Fault-tolerant spike routing algorithm and architecture for three dimensional NoC-based neuromorphic systems," IEEE Access, vol. 7, pp. 90436–90452, 2019.

[11] G. Seetharaman and D. Pati, "Reliable fault-tolerance routing technique for network-on-chip interconnect," in Intelligent Sustainable Systems, Springer, 2022, pp. 767–775.

[12] S.-C. Kao, C.-H. H. Yang, P.-Y. Chen, X. Ma, and T. Krishna, "Reinforcement learning based interconnection routing for adaptive traffic optimization," in Proceedings of the 13th IEEE/ACM International Symposium on Networks-on-Chip, 2019, pp. 1–2.

[13] M. Manzoor, R. N. Mir, and N. ud din Hakim, "PAAD (Partially adaptive and deterministic routing): A deadlock free congestion aware hybrid routing for 2D mesh network-on-chips.," Microprocessors and Microsystems, vol. 92, no. April, p. 104551, 2022, doi: 10.1016/j.micpro.2022.104551.

[14] O. S. Albahri, A. Alamleh, T. Al-Quraishi, and R. Thakkar, "Smart Real-Time IoT mHealth-based Conceptual Framework for Healthcare Services Provision during Network Failures," Applied Data Science and Analysis, vol. 2023, pp. 110–117, 2023.

[15] Y. Cai, D. Xiang, and X. Ji, "Deadlock-free adaptive 3D network-on-chips routing algorithm with repetitive turn concept," IET Communications, vol. 14, no. 11, pp. 1783–1792, 2020.

[16] S. Vazifedunn, A. Reza, and M. Reshadi, "Low-cost regional-based congestion-aware routing algorithm for 2D mesh NoC," International Journal of Communication Systems, p. e5360, 2023.

[17] Y. R. Muhsen, N. A. Husin, M. B. Zolkepli, N. Manshor, A. A. J. Al-Hchaimi, and H. M. Ridha, "Enhancing NoC-Based MPSoC performance: A predictive approach with ANN and guaranteed convergence arithmetic optimization algorithm," IEEE Access, 2023.

[18] E. A. Monakhova, O. G. Monakhov, and A. Y. Romanov, "Routing algorithms in optimal degree four circulant networks based on relative addressing: Comparative analysis for Networks-on-Chip," IEEE Transactions on Network Science and Engineering, vol. 10, no. 1, pp. 413–425, 2022.

[19] T. Patil and A. Sandi, "Design and implementation of asynchronous NOC architecture with buffer-less router," Materials Today: Proceedings, vol. 49, pp. 756–763, 2022, doi: https://doi.org/10.1016/j.matpr.2021.05.282.

[20] A. B. Gabis and M. Koudil, "NoC routing protocols–objective-based classification," Journal of Systems Architecture, vol. 66, pp. 14–32, 2016.

[21] A. Ben Achballah, S. Ben Othman, and S. Ben Saoud, "Problems and challenges of emerging technology networks− on− chip: A review," Microprocessors and Microsystems, vol. 53, pp. 1–20, 2017.

[22] N. Kadri and M. Koudil, "A survey on fault-tolerant application mapping techniques for network-on-chip," Journal of Systems Architecture, vol. 92, pp. 39–52, 2019.

[23] R. Singh et al., "Review, analysis, and implementation of path selection strategies for 2D NoCS," IEEE Access, 2022.

[24] M. Aria and C. Cuccurullo, "bibliometrix: An R-tool for comprehensive science mapping analysis," Journal of informetrics, vol. 11, no. 4, pp. 959–975, 2017.

[25] A. D. Ahmed, M. M. Salih, and Y. R. Muhsen, "Opinion Weight Criteria Method (OWCM): A New Method for Weighting Criteria with Zero Inconsistency," IEEE Access, 2024.

[26] E. A. AlOmar, M. W. Mkaouer, C. Newman, and A. Ouni, "On preserving the behavior in software refactoring: A systematic mapping study," Information and Software Technology, vol. 140, p. 106675, 2021.

[27] O. S. Albahri and A. H. AlAmoodi, "Navigating the Metaverse of Big Data: A Bibliometric Journey," Mesopotamian Journal of Big Data, vol. 2023, pp. 92–106, 2023.

[28] Y. R. Muhsen, N. A. Husin, M. B. Zolkepli, and N. Manshor, "A systematic literature review of fuzzy-weighted zero-inconsistency and fuzzy-decision-by-opinion-score-methods: assessment of the past to inform the future," Journal of Intelligent & Fuzzy Systems, no. Preprint, pp. 1–22, 2023.

[29] H. E. Khairan, S. L. Zubaidi, Y. R. Muhsen, and N. Al-Ansari, "Parameter Optimisation-Based Hybrid

Reference Evapotranspiration Prediction Models: A Systematic Review of Current Implementations and Future Research Directions," Atmosphere, vol. 14, no. 1, p. 77, 2022.

[30] M. Callon, J.-P. Courtial, W. A. Turner, and S. Bauin, "From translations to problematic networks: An introduction to co-word analysis," Social science information, vol. 22, no. 2, pp. 191–235, 1983.

[31] W. Mengist, T. Soromessa, and G. Legese, "Method for conducting systematic literature review and meta-analysis for environmental science research," MethodsX, vol. 7, p. 100777, 2020.

[32] J. Paul and A. Rosado-Serrano, "Gradual internationalization vs born-global/international new venture models: A review and research agenda," International Marketing Review, vol. 36, no. 6, pp. 830–858, 2019.

[33] N. A. Husin, A. A. Abdulsaeed, Y. R. Muhsen, A. S. Zaidan, A. Alnoor, and Z. R. Al-mawla, "Evaluation of Metaverse Tools Based on Privacy Model Using Fuzzy MCDM Approach," in International Multi-Disciplinary Conference-Integrated Sciences and Technologies, 2023, pp. 1–20.

[34] J. Paul, W. M. Lim, A. O'Cass, A. W. Hao, and S. Bresciani, "Scientific procedures and rationales for systematic literature reviews (SPAR-4-SLR)," International Journal of Consumer Studies, vol. 45, no. 4, pp. O1–O16, 2021.

[35] S. Singh and S. Dhir, "Structured review using TCCM and bibliometric analysis of international cause-related marketing, social marketing, and innovation of the firm," International Review on Public and Nonprofit Marketing, vol. 16, pp. 335–347, 2019.

[36] S. Kumar, N. Pandey, and A. Haldar, "Twenty years of Public Management Review (PMR): a bibliometric overview," Public Management Review, vol. 22, no. 12, pp. 1876–1896, 2020.

[37] S. Agarwal, R. Pandey, S. Kumar, W. Marc Lim, P. K. Agarwal, and A. Malik, "Workplace incivility: A retrospective review and future research agenda," Safety Science, vol. 158, no. February 2022, p. 105990, 2023, doi: 10.1016/j.ssci.2022.105990.

[38] B. A. Kareem, S. L. Zubaidi, N. Al-Ansari, and Y. R. Muhsen, "Review of Recent Trends in the Hybridisation of Preprocessing-Based and Parameter Optimisation-Based Hybrid Models to Forecast Univariate Streamflow."

[39] L. Zhao et al., "Depicting Developing Trend and Core Knowledge of Primary Open-Angle Glaucoma: A Bibliometric and Visualized Analysis," Frontiers in medicine, vol. 9, 2022.

[40] M. Gusenbauer and N. R. Haddaway, "Which academic search systems are suitable for systematic reviews or meta-analyses? Evaluating retrieval qualities of Google Scholar, PubMed, and 26 other resources," Research synthesis methods, vol. 11, no. 2, pp. 181–217, 2020.

[41] M. J. Page et al., "Updating guidance for reporting systematic reviews: development of the PRISMA 2020 statement," Journal of clinical epidemiology, vol. 134, pp. 103–112, 2021.

[42] J. Ali, K. N. Hussain, A. Alnoor, Y. R. Muhsen, and A. G. Atiyah, "Benchmarking Methodology of Banks Based on Financial Sustainability Using CRITIC and RAFSI Techniques," Decision Making: Applications in Management and Engineering, vol. 7, no. 1, pp. 315–341, 2024.

[43] O. S. Albahri et al., "Systematic review of real-time remote health monitoring system in triage and priority-based sensor technology: Taxonomy, open challenges, motivation and recommendations," Journal of medical systems, vol. 42, pp. 1–27, 2018.

[44] F. Bahman, A. Reza, M. Reshadi, and S. Vazifedan, "CACBR: Congestion Aware Cluster Buffer base routing algorithm with minimal cost on NOC," CCF Transactions on High Performance Computing, vol. 2, no. 3, pp. 297–306, 2020, doi: 10.1007/s42514-020-00027-8.

[45] L. Wang, X. Wang, and T. Mak, "Adaptive routing algorithms for lifetime reliability optimization in network-on-chip," IEEE Transactions on Computers, vol. 65, no. 9, pp. 2896–2902, 2015.

[46] M. Li, Q.-A. Zeng, and W.-B. Jone, "DyXY: a proximity congestion-aware deadlock-free dynamic routing method for network on chip," in Proceedings of the 43rd annual Design Automation Conference, 2006, pp. 849–852.

[47] A. A. J. Al-Hchaimi, W. N. Flayyih, F. Hashim, M. S. Rusli, and F. Z. Rokhani, "Review of 3D Networks-On-Chip Simulators and Plugins," in 2021 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia), 2021, pp. 17–20, doi: 10.1109/PrimeAsia51450.2021.9701472.

[48] J. Kim, D. Park, T. Theocharides, N. Vijaykrishnan, and C. R. Das, "A low latency router supporting adaptivity for on-chip interconnects," in Proceedings of the 42nd annual Design Automation Conference, 2005, pp. 559–564.

[49] P. Gratz, B. Grot, and S. W. Keckler, "Regional congestion awareness for load balance in networks-on-chip," in 2008 IEEE 14th International Symposium on High Performance Computer Architecture, 2008, pp. 203–214.

[50] S. Ma, N. E. Jerger, and Z. Wang, "DBAR: An efficient routing algorithm to support multiple concurrent applications in networks-on-chip," Proceedings - International Symposium on Computer Architecture, pp. 413–424, 2011, doi: 10.1145/2000064.2000113.

[51] M. Ebrahimi, M. Daneshtalab, P. Liljeberg, J. Plosila, and H. Tenhunen, "CATRA-congestion aware trapezoid-based routing algorithm for on-chip networks," in 2012 Design, Automation & Test in Europe Conference & Exhibition (DATE), 2012, pp. 320–325.

[52] A. Menon, L. Zeng, X. Jiang, and T. Watanabe, "Adaptive Look Ahead Algorithm for 2-D Mesh NoC," in 2015 IEEE International Advance Computing Conference (IACC), 2015, pp. 299–302.

[53] E.-J. Chang, C.-H. Chao, K.-Y. Jheng, H.-K. Hsin, and A.-Y. Wu, "ACO-based cascaded adaptive routing for traffic balancing in NoC systems," in The 2010 International Conference on Green Circuits and Systems, 2010, pp. 317–322.

[54] C. Wang, W.-H. Hu, and N. Bagherzadeh, "Scalable load balancing congestion-aware Network-on-Chip router architecture," Journal of computer and system sciences, vol. 79, no. 4, pp. 421–439, 2013.

[55] S. Xu, B. Fu, M. Chen, and L. Zhang, "Congestion-aware adaptive routing with quantitative congestion information," in 2016 IEEE 18th International Conference on High Performance Computing and Communications; IEEE 14th International Conference on Smart City; IEEE 2nd International Conference on Data Science and Systems (HPCC/SmartCity/DSS), 2016, pp. 216–223.

[56] M. Ramakrishna, V. K. Kodati, P. V Gratz, and A. Sprintson, "GCA: Global congestion awareness for load balance in networks-on-chip," IEEE Transactions on Parallel and Distributed Systems, vol. 27, no. 7, pp. 2022–2035, 2015.

[57] B. Fu and J. Kim, "Footprint: Regulating routing adaptiveness in networks-on-chip," in Proceedings of the 44th Annual International Symposium on Computer Architecture, 2017, pp. 691–702.

[58] K. Tatas and C. Chrysostomou, "Adaptive Networks-on-Chip Routing with Fuzzy Logic Control," in 2016 Euromicro Conference on Digital System Design (DSD), 2016, pp. 138–145.

[59] K. Gaffour, M. K. Benhaoua, A. H. Benyamina, and H.-E. Zahaf, "A new congestion-aware routing algorithm in network-on-chip: 2D and 3D comparison," International Journal of Computers and Applications, vol. 45, no. 1, pp. 27–35, 2023.

[60] S. Höppner et al., "An energy efficient multi-Gbit/s NoC transceiver architecture with combined AC/DC drivers and stoppable clocking in 65 nm and 28 nm CMOS," IEEE Journal of Solid-State Circuits, vol. 50, no. 3, pp. 749–762, 2015.

[61] H. C. Touati and F. Boutekkouk, "FACARS: A novel fully adaptive congestion aware routing scheme for network on chip," in 2018 7th Mediterranean Conference on Embedded Computing (MECO), 2018, pp. 1–6.

[62] D. Deb, J. Jose, S. Das, and H. K. Kapoor, "Cost effective routing techniques in 2D mesh NoC using on-chip transmission lines," Journal of Parallel and Distributed Computing, vol. 123, pp. 118–129, 2019, doi: 10.1016/j.jpdc.2018.09.009.

[63] A. Javed, J. Harkin, L. McDaid, and J. Liu, "Exploring spiking neural networks for prediction of traffic congestion in networks-on-chip," in 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, pp. 1–5.

[64] Y. Luo, M. C. Meyer, X. Jiang, and T. Watanabe, "A hotspot-pattern-aware routing algorithm for networks-on-chip," in 2019 IEEE 13th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC), 2019, pp. 229–235.

[65] S. Mikaeeli Mamaghani and M. A. Jabraeil Jamali, "A load-balanced congestion-aware routing algorithm based on time interval in wireless network-on-chip," Journal of Ambient Intelligence and Humanized Computing, vol.

10, no. 7, pp. 2869–2882, 2019, doi: 10.1007/s12652-018-1020-z.

[66] A. Javed, J. Harkin, L. McDaid, and J. Liu, “Minimising Impact of Local Congestion in Networks-on-Chip Performance by Predicting Buffer Utilisation,” in 2020 31st Irish Signals and Systems Conference (ISSC), 2020, pp. 1–6.

[67] R. Akbar and F. Safaei, “A novel congestion-aware routing algorithm with prediction in mesh-based networks-on-chip,” Nano Communication Networks, vol. 26, p. 100322, 2020, doi: 10.1016/j.nancom.2020.100322.

[68] W. Zong, M. O. Agyemen, X. Wang, and T. Maky, “Unbiased regional congestion aware selection function for nocs,” in Proceedings of the 9th International Symposium on Networks-on-Chip, 2015, pp. 1–8.

[69] H. C. Touati and F. Boutekkouk, “A weighted minimal fully adaptive congestion aware routing algorithm for network on chip,” in 2017 First International Conference on Embedded & Distributed Systems (EDiS), 2017, pp. 1–5.

[70] R. Akbar and F. Safaei, “A novel heterogeneous congestion criterion for mesh-based networks-on-chip,” Microprocessors and Microsystems, vol. 84, no. December 2020, p. 104056, 2021, doi: 10.1016/j.micpro.2021.104056.

[71] M. Trik, A. M. N. G. Molk, F. Ghasemi, and P. Pouryeganeh, “A hybrid selection strategy based on traffic analysis for improving performance in networks on chip,” Journal of Sensors, vol. 2022, 2022.

[72] H.-K. Hsin, E.-J. Chang, K.-Y. Su, and A.-Y. Wu, “Ant colony optimization-based adaptive network-on-chip routing framework using network information region,” IEEE Transactions on Computers, vol. 64, no. 8, pp. 2119–2131, 2014.

[73] R. S. Reshma Raj, C. Gayathri, S. Kalady, and P. B. Jayaraj, “Odd-even based adaptive two-way routing in mesh NoCs for hotspot mitigation,” in Proceedings of the 20th International Conference on Distributed Computing and Networking, 2019, pp. 248–252.

[74] M. A. Yazdi, M. Modarressi, and H. Sarbazi-Azad, “A load-balanced routing scheme for noc-based systems-on-chip,” in 2010 First Workshop on Hardware and Software Implementation and Control of Distributed MEMS, 2010, pp. 72–77.

[75] M. Kumar, V. Laxmi, M. S. Gaur, M. Daneshtalab, and M. Zwolinski, “A novel non-minimal turn model for highly adaptive routing in 2D NoCs,” in 2014 22nd International Conference on Very Large Scale Integration (VLSI-SoC), 2014, pp. 1–6.

[76] H. Zhu, P. P. Pande, and C. Grecu, “Performance evaluation of adaptive routing algorithms for achieving fault tolerance in NoC fabrics,” in 2007 IEEE International Conf. on Application-specific Systems, Architectures and Processors (ASAP), 2007, pp. 42–47.

[77] J. Domke, T. Hoefler, and S. Matsuoka, “Routing on the dependency graph: A new approach to deadlock-free high-performance routing,” in proceedings of the 25th ACM international symposium on high-performance parallel and distributed computing, 2016, pp. 3–14.

[78] G. Oxman and S. Weiss, “Deflection Routing in Hierarchical Mesh NoCs,” IEEE Embedded Systems Letters, vol. 8, no. 2, pp. 45–48, 2016.

[79] D. R. G. Silva, B. S. Oliveira, and F. G. Moraes, “Effects of the NoC architecture in the performance of NoC-based MPSoCs,” in 2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2014, pp. 431–434.

[80] M. Jalili, J. Bourgeois, and H. Sarbazi-Azad, “Power-efficient partially-adaptive routing in on-chip mesh networks,” in 2016 International SoC Design Conference (ISOCC), 2016, pp. 65–66.

[81] K. Nasiri and H. R. Zarandi, “MWPF: A Deadlock Avoidance Fully Adaptive Routing Algorithm in Networks-on-Chip,” in 2016 24th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP), 2016, pp. 734–741.

[82] K. Tan, H. Liu, J. Zhang, Y. Zhang, J. Fang, and G. M. Voelker, “Sora: high-performance software radio using general-purpose multi-core processors,” Communications of the ACM, vol. 54, no. 1, pp. 99–107, 2011.

[83] N. Wang and P. Valencia, “Traffic Allocation: An efficient adaptive network-on-chip routing algorithm design,” in 2016 2nd IEEE International Conference on Computer and Communications (ICCC), 2016, pp.

2015–2019.

[84] E. Fusella and A. Cilardo, “Lattice-based turn model for adaptive routing,” IEEE Transactions on Parallel and Distributed Systems, vol. 29, no. 5, pp. 1117–1130, 2017.

[85] N. Rohbani, Z. Shirmohammadi, M. Zare, and S.-G. Miremadi, “LAXY: A location-based aging-resilient Xy-Yx routing algorithm for network on chip,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 36, no. 10, pp. 1725–1738, 2017.

[86] M. Tang, X. Lin, and M. Palesi, “The repetitive turn model for adaptive routing,” IEEE Transactions on Computers, vol. 66, no. 1, pp. 138–146, 2016.

[87] A. Charif, A. Coelho, N.-E. Zergainoh, and M. Nicolaidis, “MINI-ESPADA: A low-cost fully adaptive routing mechanism for Networks-on-Chips,” in 2017 18th IEEE Latin American Test Symposium (LATS), 2017, pp. 1–4.

[88] P. Valencia, E. Muller, and N. Wang, “ZigZag: An efficient deterministic Network-on-chip routing algorithm design,” in 2017 8th IEEE Annual Information Technology, Electronics and Mobile Communication Conference (IEMCON), 2017, pp. 1–5.

[89] S. Y. Jiang, G. Luo, Y. Liu, S. S. Jiang, and X. T. Li, “Fault-tolerant routing algorithm simulation and hardware verification of NoC,” IEEE Transactions on Applied Superconductivity, vol. 24, no. 5, pp. 1–5, 2014.

[90] J. Cardona, C. Hernandez, J. Abella, and F. J. Cazorla, “EOmesh: combined flow balancing and deterministic routing for reduced WCET estimates in embedded real-time systems,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 37, no. 11, pp. 2451–2461, 2018.

[91] V. Pano, S. Lerner, I. Yilmaz, M. Lui, and B. Taskin, “Workload-aware routing (WAR) for network-on-chip lifetime improvement,” in 2018 IEEE International Symposium on Circuits and Systems (ISCAS), 2018, pp. 1–5.

[92] S. Umapathy, M. Shah, and N. Wang, “Encircle routing: An efficient deterministic network on chip routing algorithm,” in 2018 IEEE 8th Annual Computing and Communication Workshop and Conference (CCWC), 2018, pp. 895–899.

[93] W. Zhang, L. Hou, J. Wang, S. Geng, and W. Wu, “Comparison research between xy and odd-even routing algorithm of a 2-dimension 3x3 mesh topology network-on-chip,” in 2009 WRI Global Congress on Intelligent Systems, 2009, vol. 3, pp. 329–333.

[94] A. Jain, V. Laxmi, M. Tripathi, M. S. Gaur, and R. Bishnoi, “TRACK: An algorithm for fault-tolerant, dynamic and scalable 2D mesh network-on-chip routing reconfiguration,” Integration, vol. 72, pp. 92–110, 2020.

[95] K. Wang and A. Louri, “Cure: A high-performance, low-power, and reliable network-on-chip design using reinforcement learning,” IEEE Transactions on Parallel and Distributed Systems, vol. 31, no. 9, pp. 2125–2138, 2020.

[96] S. T. Muhammad, M. Saad, A. A. El-Moursy, M. A. El-Moursy, and H. F. A. Hamed, “CFPA: Congestion aware, fault tolerant and process variation aware adaptive routing algorithm for asynchronous Networks-on-Chip,” Journal of Parallel and Distributed Computing, vol. 128, pp. 151–166, 2019, doi: https://doi.org/10.1016/j.jpdc.2019.03.001.

[97] X. Xu and D. Guo, “Hierarchical routing architecture (HRA),” in 2008 Next Generation Internet Networks, 2008, pp. 92–99.

[98] J. Flich and J. Duato, “Logic-based distributed routing for NoCs,” IEEE computer architecture letters, vol. 7, no. 1, pp. 13–16, 2008.

[99] I. Gojmerac, T. Ziegler, F. Ricciato, and P. Reichl, “Adaptive multipath routing for dynamic traffic engineering,” in GLOBECOM’03. IEEE Global Telecommunications Conference (IEEE Cat. No. 03CH37489), 2003, vol. 6, pp. 3058–3062.